**ECEN 248 - Lab Report**

**Lab Number: 3**

**Lab Title: Rudimentary Adder Circuits**

**Section Number: 519**

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**Objectives:**

The purpose of this lab is to design various adders with digital logic gates. Starting with a half-adder, and working towards a 2-bit ripple carry adder.

**Design:**

Using the schematic from the prelab design a half-adder. Checking the design and logic with the Lab 3 Slide, verify the half adder by outputting the Sum and Carry out to two LEDs. Create a full-adder, using the full-adder design from the prelab. Using two LEDs, to verify the logic. Create the 2-bit ripple carry adder, using the design from the prelab. Use three LEDs to check the Sum 1, Sum 2, and the Carry out.

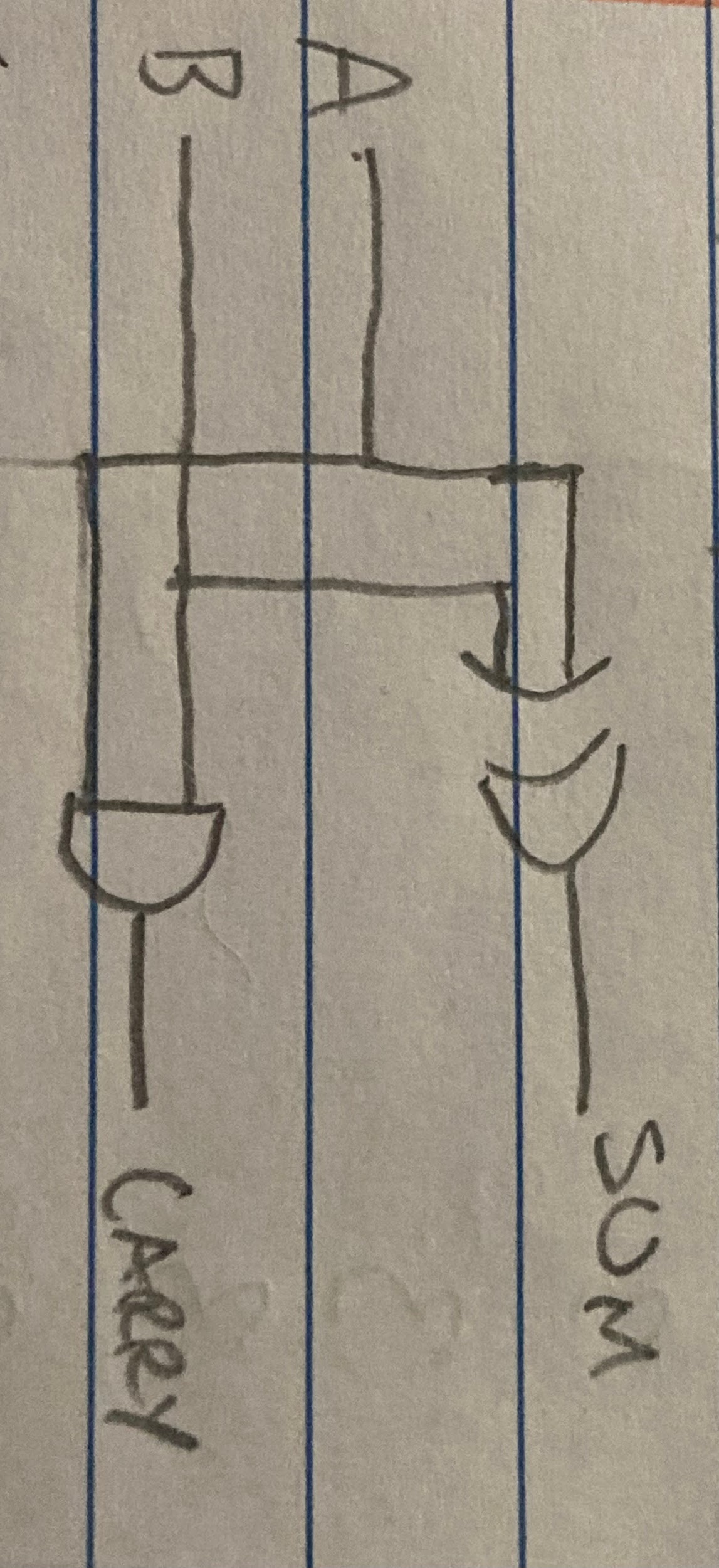
**Conclusion:**

In this lab, I built different adders. From a half-adder to a 2-bit ripple carry adder. Using LEDs to test the logic of the adder designs found in the prelab. The designs worked; however, one source of error was certain logic gates pins were not working properly.

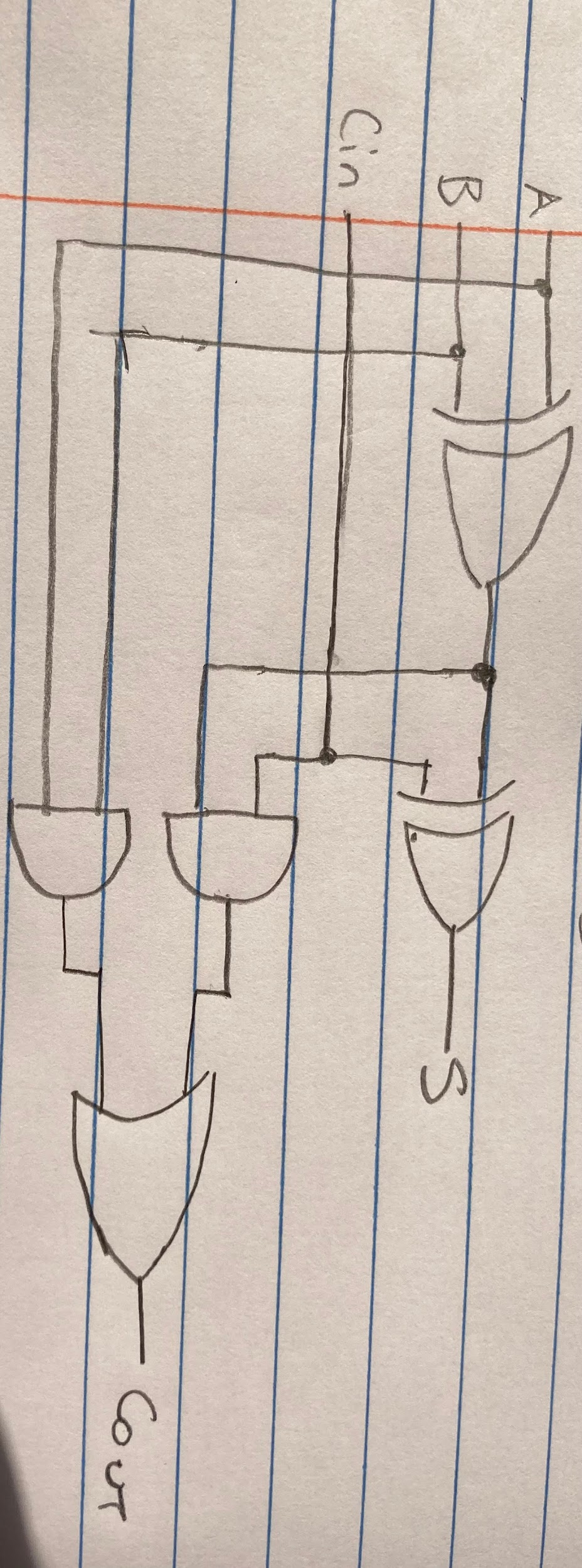
**Post-lab Deliverables:**

1. The Full-Adder used in the prelab did not function during the lab. A new design was used, this new design’s schematic is shown below.

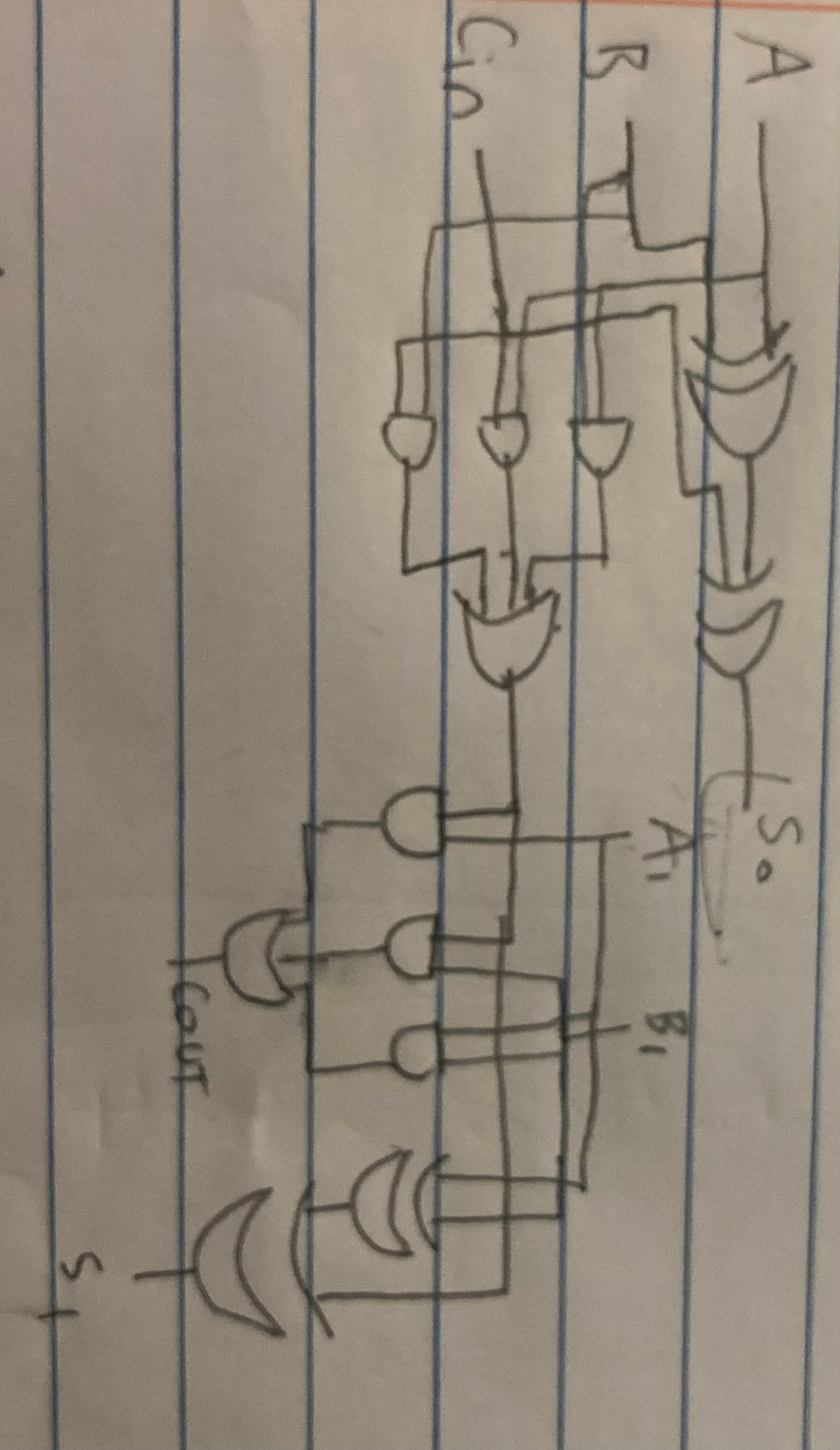
Half-Adder Design:



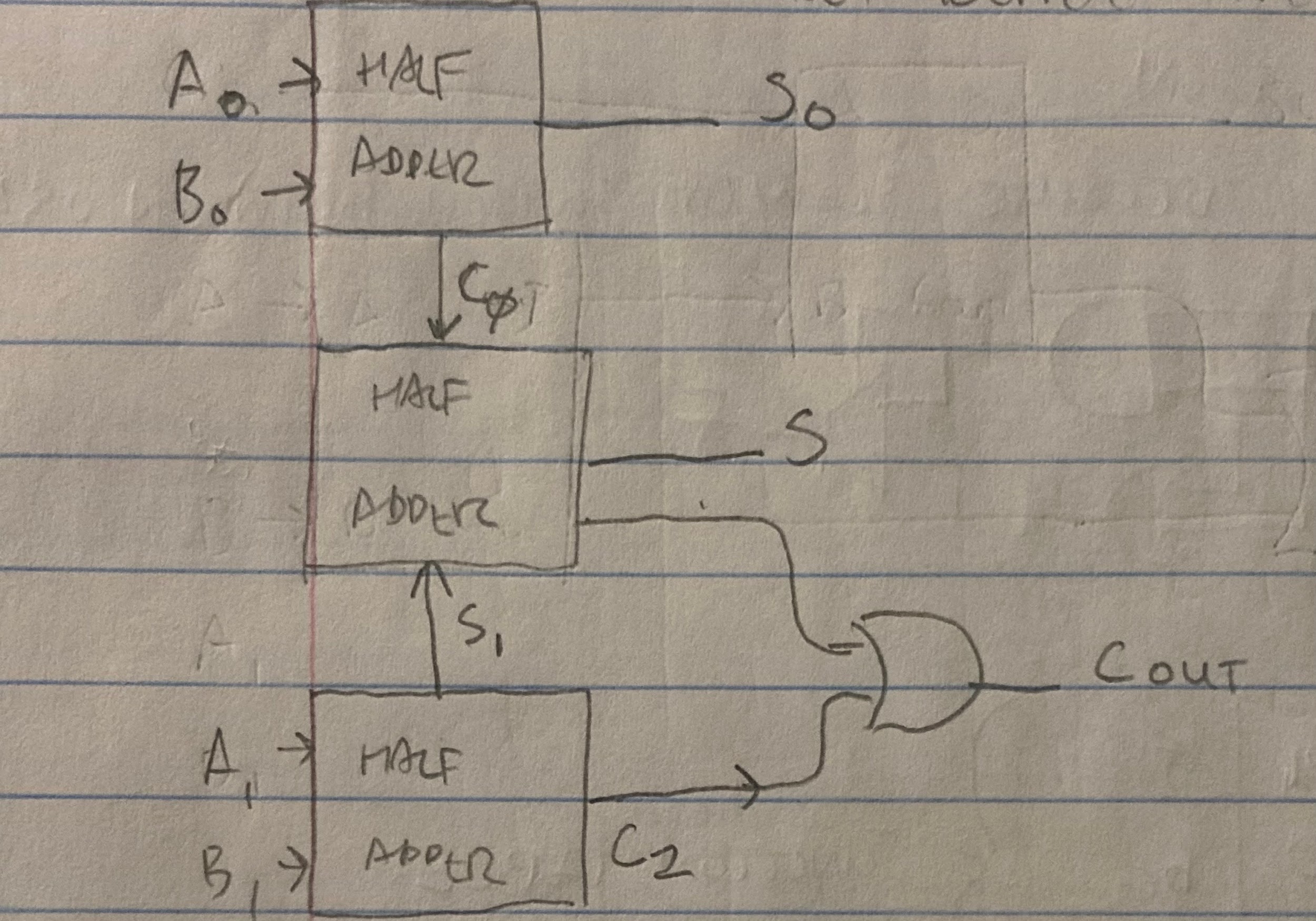
Full-Adder Design:



2-bit Ripple Carry Adder



1. The worst propagation delay for the full adder design assuming each gate has the same delay of 1 unit, is 3. This path is from the A XOR B output to the AND gate with Cin, to the OR gate resulting in the Cout value.
2. A 2-bit Ripple Carry Adder design with half-adder circuits and OR gates:



Feedback:

* Some of the ICs have only a few functional pins, which results in testing all pins of a logic gate before using or having to use more than the required amount of IC to design the circuit.